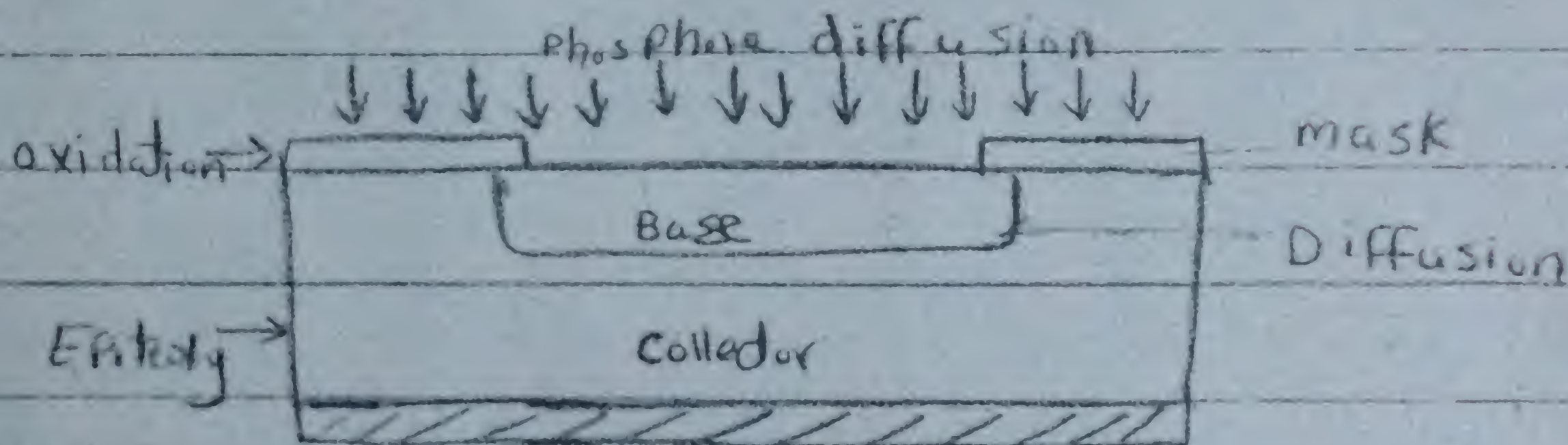


## Question: 4

steps to fabricate a BJT:

1. A lightly doped layer of  $n$ -type material is epitaxially grown on a  $p^+$  wafer. The  $n$ -s.c. will constitute the collector material, the  $p^+$  support can be used to provide efficient device isolation when the device is used in IC. This isolation can be achieved by applying a strong -ve bias to the  $p^+$  s.c.

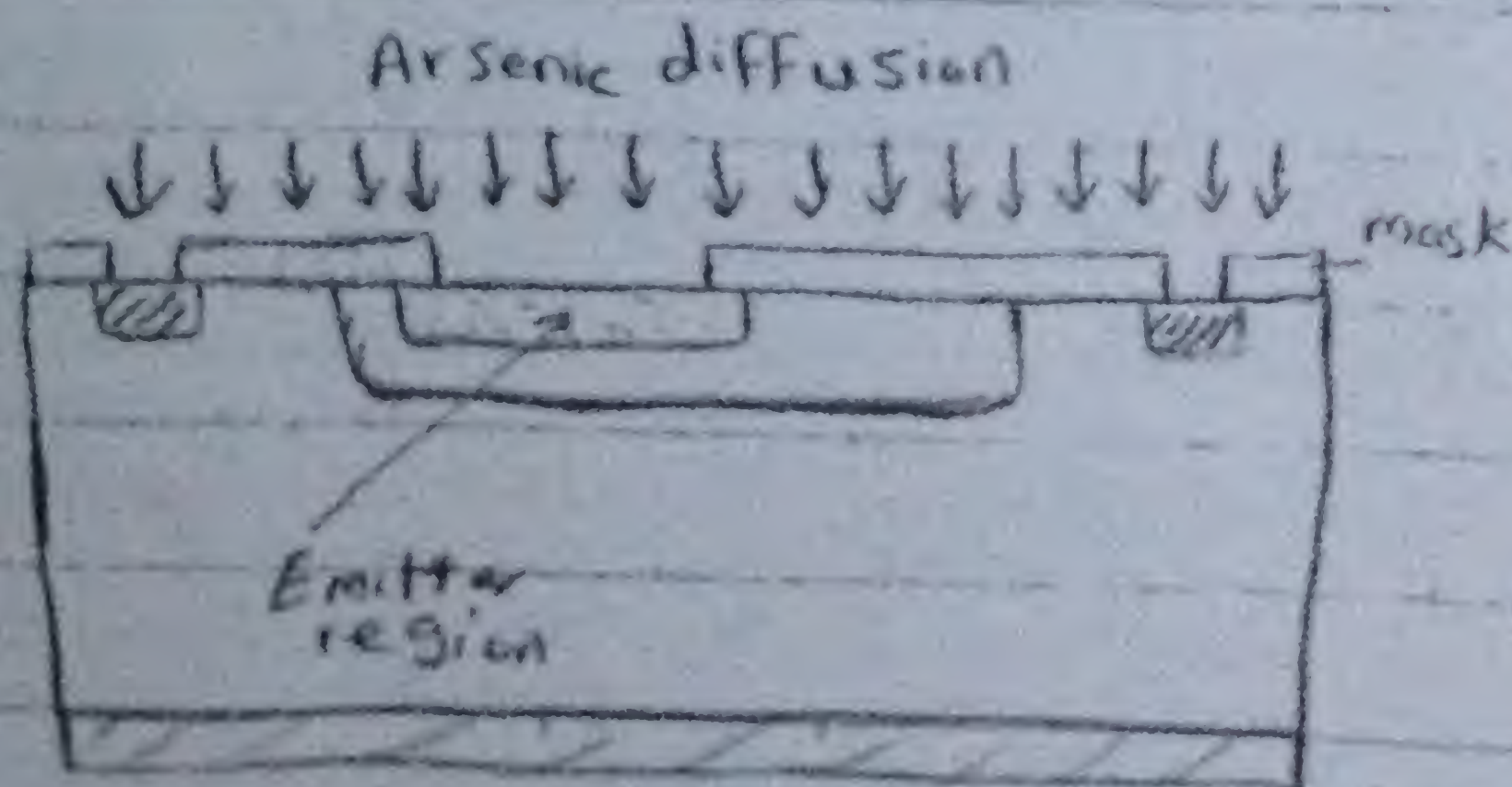
2. The wafer surface is oxidized, and using photolithographic step to create the appropriate mask, a  $p$ -layer (the base region) is diffused in the  $n$ -material.



3. The oxide layer is stripped away and a new layer is grown, usually by wet oxidation process.

4. Using photolithography, another mask is created that exposes the s.c. material at the proper positions for diffusion of the emitter and of the collector contact regions.

5. By either diffusion or ion implantation, shallow heavily doped  $n$  and  $n^+$  regions are fabricated, they are the emitter and ohmic contact regions of the collector.



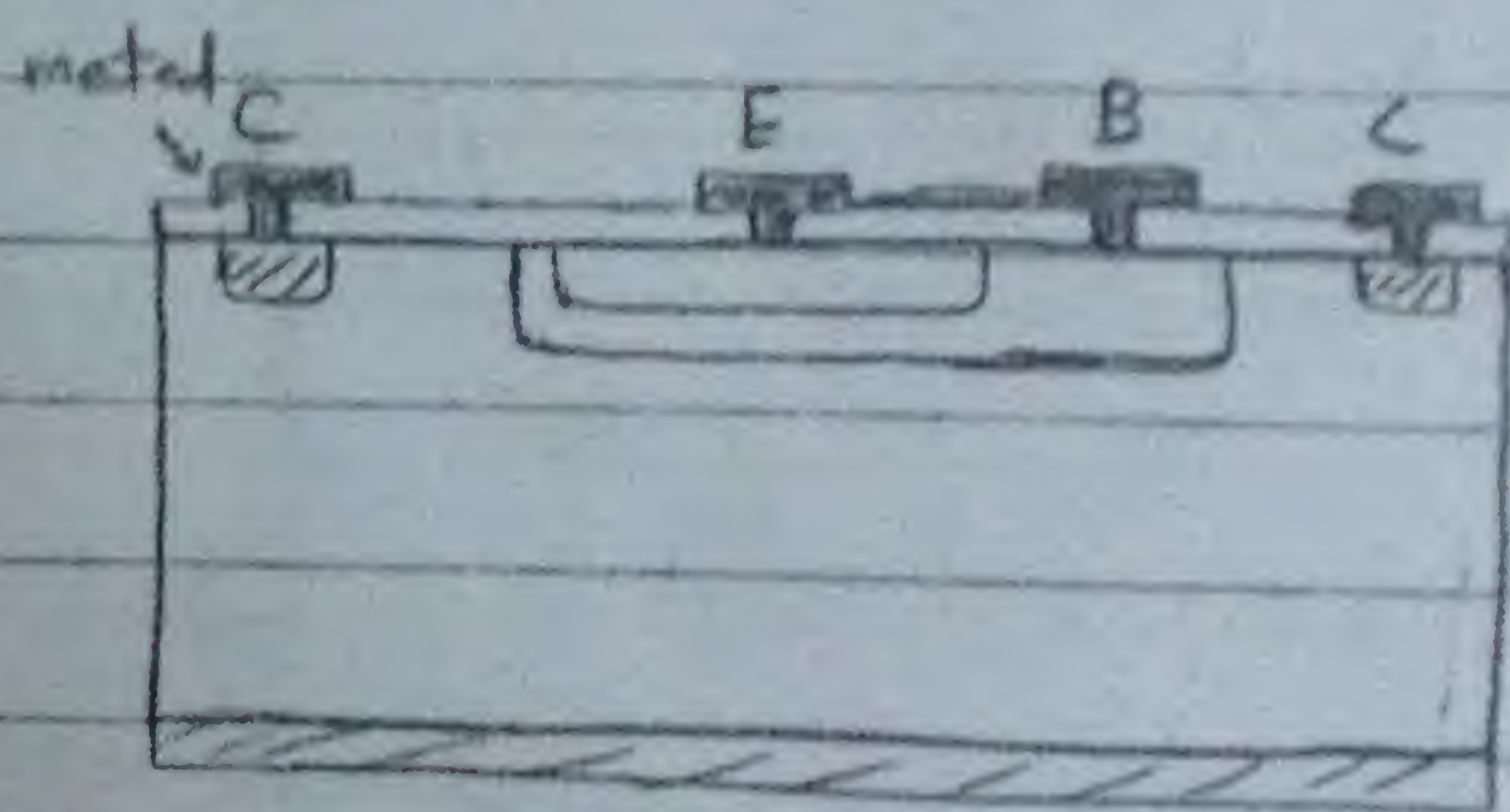


(11)

11

the oxide layer is stripped away and a new oxide coating is grown, then using photolithography another mask is created that have wells opened in the oxide to permit contact with the various regions of the transistor

7. the whole face of the wafer is metallized and using another mask, the metal is etched to yield the desired electrode configuration. show in the figure below.



Question: 5

(1) CMOS inverter

- when a HIGH is applied to the i/p,  $Q_1$  is off and  $Q_2$  is on, this condition connects the o/p to ground through the <sup>on</sup> resistance of  $Q_2$  resulting in a Low o/p

- when a Low is applied to the i/p,  $Q_1$  is on and  $Q_2$  is off, this condition connects the o/p to  $+V_{DD}$  through the on resistance of  $Q_1$  resulting in a high o/p

